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LISTING OF CLAIMS

1. (Currently amended) A method of fabricating a semiconductor device comprising the steps of:
forming a gate dielectric layer on a semiconductor substrate;
forming a gate electrode over the gate dielectric layer wherein the gate electrode defines a channel interposed between source/drain regions formed within an active region of the semiconductor substrate; and
forming contact etch resistant spacers on sidewalls of the gate electrode and sidewalls of the gate dielectric layer, the contact etch resistant spacers being of a non-silicon oxide and a non-nitride material; and
forming a liner layer over the contact etch resistant spacers of at least one of Si_3N_4 and SiO_2N_2 .
2. (Original) The method according to claim 1, wherein the step of forming the contact etch resistant spacers includes the steps of:
forming a contact etch resistant layer on the sidewalls of the gate electrode, the sidewalls of the gate dielectric and portions of the upper surface of the semiconductor substrate; and
etching the contact etch resistant layer to form the contact etch resistant spacers.
3. (Original) The method of claim 2, further including the step of:
forming the contact etch resistant layer of at least one of silicon carbide and undoped silicon.
4. (Canceled)

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5. (Currently amended) The method of claim 1, further including the step of: forming ~~[[an]]~~ a silicon-oxide interlevel dielectric layer over the liner layer contact ~~etch-resistant spacers of SiO_x.~~

6. (Original) The method of claim 5, further including the step of: forming a contact mask over the interlevel dielectric layer; and etching a contact aperture to expose a source/drain region.

7-20. (Canceled)

21. (New) A method of fabricating a semiconductor device comprising:
forming a gate dielectric layer on a semiconductor substrate;
forming a gate electrode over the gate dielectric layer wherein the gate electrode defines a channel interposed between source/drain regions formed within an active region of the semiconductor substrate;
forming contact etch resistant spacers on sidewalls of the gate electrode, the contact etch resistant spacers being of a non-silicon oxide material and a non-silicon nitride material; and
forming a nitrogen containing dielectric material liner layer over the contact etch resistant spacers.

22. (New) The method of claim 21, wherein forming the contact etch resistant spacers includes forming a contact etch resistant layer on the sidewalls of the gate electrode and etching the contact etch resistant layer to form the contact etch resistant spacers.

23. (New) The method of claim 21, wherein the contact etch resistant spacers are silicon carbide.

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24. (New) The method of claim 21, wherein the contact etch resistant spacers are undoped silicon.
25. (New) The method of claim 21, further comprising forming an interlevel dielectric layer over the liner layer, forming a contact mask over the interlevel dielectric layer and etching a contact aperture to expose a source/drain region.
26. (New) The method of claim 25, wherein the etching a contact aperture includes etching a portion of the interlevel dielectric layer and a portion of the liner layer.
27. (New) The method of claim 21, wherein the liner layer is one of silicon nitride or silicon oxynitride.
28. (New) A method of fabricating a semiconductor device, comprising:
forming a gate dielectric layer on a semiconductor substrate;
forming a gate electrode over the gate dielectric layer wherein the gate electrode defines a channel interposed between source/drain regions formed within an active region of the semiconductor substrate;
forming spacers on sidewalls of the gate electrode, the spacers having etch selectivity with respect to silicon oxide and silicon nitride;
forming an interlevel dielectric layer over the gate electrode and the spacers;
forming a contact mask over the interlevel dielectric layer;
etching a contact aperture to simultaneously expose one of the source or the drain and at least a portion of an adjacent spacer; and
filling the contact aperture with a conductive material to form a contact that is electrically coupled to the one of the source or drain and is electrically isolated from the gate electrode, the contact touching the spacer in the portion exposed by the etching and the spacer providing physical and electrical isolation between the contact and the gate electrode.

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29. (New) The method of claim 28, wherein forming the spacers includes:
forming a spacer material layer on the sidewalls of the gate electrode, the
sidewalls of the gate dielectric and portions of the upper surface of the semiconductor
substrate; and
etching the spacer material layer to form the spacers.
30. (New) The method of claim 28, wherein the spacers are silicon carbide.
31. (New) The method of claim 28, wherein the spacers are undoped silicon.
32. (New) The method of claim 28, further including forming a silicon nitride
liner layer between the spacers and the interlevel dielectric layer.
33. (New) The method of claim 28, further including forming a silicon
oxynitride liner layer between the spacers and the interlevel dielectric layer.
34. (New) The method of claim 28, wherein the spacers have a width of
between 200 angstroms and 400 angstroms.
35. (New) The method of claim 28, further including forming a liner layer of a
nitrogen containing dielectric material between the spacers and the interlevel dielectric
layer, and the etching a contact aperture includes etching a portion of the interlevel
dielectric layer and a portion of the liner layer